Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. – 80. (cancelled.)

81-82. (canceled)

83. (previously presented) A method of erasing a MONOS memory cell, wherein said MONOS memory cell comprises:

a word gate on the surface of a semiconductor substrate;

sidewall control gates on sidewalls of said word gate, separated from said word gates by an insulating layer;

nitride regions within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions;

a polysilicon word line overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and

bit line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates;

wherein said method of erasing a block of said nitride regions comprises the steps of:

providing a first voltage to said bit line diffusions; and

providing a second voltage opposite to said first voltage to said control gate over said bit line diffusions.

84. – 86. (cancelled.)

87-93. (canceled)

94. (new) The method according to Claim 83 wherein said first voltage is a positive voltage and wherein said second voltage is a negative voltage.

95. (new) The method according to Claim 83 said first voltage is a negative voltage wherein said negative voltage is also applied to said semiconductor substrate and wherein said second voltage is a positive voltage.